Bi-weekly Status Report 4
Senior Design, December 2020, Team 14

Introduction of Real-World Signals and Systems into ECpE DSP Laboratory Curriculum

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Progress Summary:
This week we finished the first beta of the front end GUI, completed interrupt-based firmware beta, validated DAC and ADC designs, rolled these designs in to the main board, began drafts for multiple labs, validated two lab designs, worked on documentation, completed one lab, and began mechanical design for two additional labs.

Individual Contributions by Team Member:

- **Brady Anderson (Biweekly: 20; Cumulative: 130)**
  - Completed interrupt-based firmware architecture
  - Cleaned up firmware code, unified design schema
  - Integrated AXI Quad SPI controller into FPGA fabric
    - Began configuring SPI controller from PS
- **Sam Burnett (Bi-weekly: 25, Cumulative: 146)**
  - Built data converters EVM
  - Tested DAC with SPI communication
  - Tested ADC with SPI communication
  - Finished anti-aliasing filter design
  - Updated main PCB layout
    - Condensed PMIC block
    - Integrated DAC design
    - Integrated ADC design
- **Mitchell Hoppe (Weekly: 12; Cumulative: 110.0)**
  - Updated the MATLAB gui to include the feedback that was given in the first demo.
  - Demoed the GUI to the group and our advisor to show what progress has been made over the last year.
  - Added last-minute quality-of-life improvements to the GUI.
- **Max Kiley (Biweekly: 115; Cumulative: 126)**
  - Began drafting Lab 1 for EE 324
  - Continued simulating LC circuit for lab 1
  - Planned a mechanical spring-mass-damper system for lab 1
- **Emily LaGrant (Biweekly: 12; Cumulative: 115)**
  - Begin drafting final power project lab
  - Work on documentation
  - Finish drafting image restoration lab

- **Isaac Rex (Bi-Weekly: 14; Cumulative: 180)**
    - Completed all design concepts for controls lab I
    - Finished writing controls lab I
    - Began developing mechanical system for controls lab II
    - Began research on sensor modeling for Simulink controller design

Pending Issues:

- Fabrication of data acquisition evaluation board is challenging (small packages)
- Signal path and SPI communication functionality needs to be tested off system
- Live streaming of data to lab PCs may require some firmware design changes. UART RX process is polled but may also need to transmit periodically, necessitating a timeout or hybrid FreeRTOS approach
- UART cannot keep up with 1 MHz+ ADC sample rates, so some buffering will be necessary. Sliding R/W heads would maximize buffer utilization

Plans:

- Isaac:
    - Adapt Labview script to work with DAD
    - Finish mechanical design prototype for controls lab II
    - Create Simulink model for distance sensor
- Emily:
    - Begin work on power control lab
    - Continue testing image restoration lab
    - Work on faculty demo of CyDAQ
    - Work on PIRM presentation
- Brady:
    - Implement SPI controller setup in PS
    - Test SPI controller with DAC eval module
    - Investigate possible solutions for UART streaming mode
- Sam:
    - Complete fabrication documentation for assembly house
    - Hold design review for the new rev of main PCB
    - Order new revision of main PCB with integrated designs
- Max
    - Order parts for spring-mass-damper system and build a prototype
    - Continue working on lab documentation for lab 1.
- Mitch
    - Change the sampling mode on the Front end and the CyDaq to streaming mode, so we can fetch the samples as they arrive. Instead of all at once at the end of the sampling period.
    - Have the Matlab front end automatically add the python scripts to the User PATH of windows if it is not already there.